

**TERMINAL ASSIGNMENT**

## CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

High-Voltage Types (20-Volt Rating)

**Features:**

- Independence of power-supply sequence considerations— $V_{CC}$  can exceed  $V_{DD}$ ; input signals can exceed both  $V_{CC}$  and  $V_{DD}$
- Up and down level-shifting capability
- Shiftable input threshold for either CMOS or TTL compatibility
- Standardized symmetrical output characteristics
- 100% tested for quiescent current @ 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5 V, 10 V, and 15 V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4504B hex voltage level-shifter consists of six circuits which shift input signals from the  $V_{CC}$  logic level to the  $V_{DD}$  logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the  $V_{CC}$  HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

The CD4504B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and MT suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

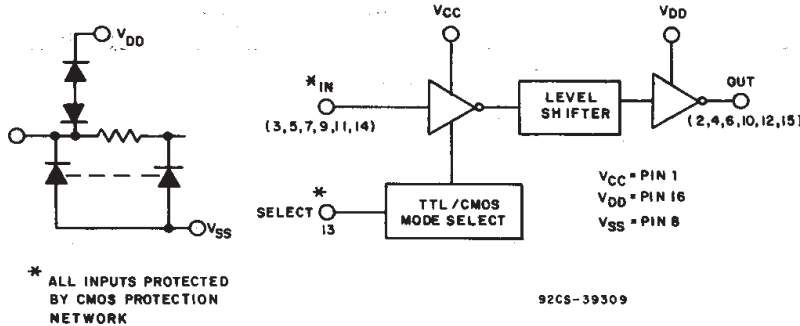


Fig. 1 - Functional diagram for CD4504B.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

|  |  |
|--|--|
| <b>DC SUPPLY-VOLTAGE RANGE, (<math>V_{DD}</math>)</b>                      |  |
| Voltages referenced to $V_{SS}$ Terminal                                   | -0.5V to +20V                                      |
| <b>INPUT VOLTAGE RANGE, ALL INPUTS</b>                                     |  |
|  | -0.5V to $V_{CC}$ +0.5V                            |
| <b>DC INPUT CURRENT, ANY ONE INPUT</b>                                     |  |
|  | $\pm$ 10mA   |
| <b>POWER DISSIPATION PER PACKAGE (<math>P_D</math>):</b>                   |  |
| For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$                      | 500mW  |
| For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ :                   | Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW |
| <b>DEVICE DISSIPATION PER OUTPUT TRANSISTOR -</b>                          |  |
| FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)             | 100mW  |
| <b>OPERATING-TEMPERATURE RANGE (<math>T_A</math>)</b>                      |  |
|  | -55°C to +125°C                                    |
| <b>STORAGE TEMPERATURE RANGE (<math>T_{stg}</math>)</b>                    |  |
|  | -85°C to +150°C                                    |
| <b>LEAD TEMPERATURE (DURING SOLDERING):</b>                                |  |
| At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max | +265°C   |

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4504B Types

V<sub>GEN</sub>

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC  | CONDITIONS            |                        |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |   |
|---|-----------------------|------------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|---|
|   | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>CC</sub><br>(V) | V <sub>DD</sub><br>(V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |   |
|   |                       |                        |                        |                        |                                       |       |       |       | MIN   | TYP               | MAX  |       |   |
| Quiescent Device Current, I <sub>DD</sub> Max and I <sub>CC</sub> in CMOS-CMOS Mode | —                     | 0,5                    | 5                      | 5                      | 1.5                                   | 1.5   | 1.5   | 1.5   | —     | 0.02              | 1.5  | mA    |   |
|   | —                     | 0,10                   | 5                      | 10                     | 2                                     | 2     | 2     | 2     | —     | 0.02              | 2    |       |   |
|   | —                     | 0,15                   | 5                      | 15                     | 4                                     | 4     | 120   | 120   | —     | 0.02              | 4    | μA    |   |
|   | —                     | 0,20                   | 5                      | 20                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |   |
| Quiescent Device Current, I <sub>CC</sub> Max TTL-CMOS Mode                         | —                     | 0,5                    | 5                      | 5                      | 5                                     | 5     | 6     | 6     | —     | 2.5               | 5    | mA    |   |
|   | —                     | 0,10                   | 5                      | 10                     | 5                                     | 5     | 6     | 6     | —     | 2.5               | 5    |       |   |
|   | —                     | 0,15                   | 5                      | 15                     | 5                                     | 5     | 6     | 6     | —     | 2.5               | 5    |       |   |
| Output Low (Sink) Current, I <sub>OL</sub> Min                                      | 0.4                   | 0.5                    | —                      | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |   |
|   | 0.5                   | 0,10                   | —                      | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |   |
|   | 1.5                   | 0,15                   | —                      | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |   |
| Output High (Source) Current, I <sub>OH</sub> Min                                   | 4.6                   | 0,5                    | —                      | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |   |
|   | 2.5                   | 0,5                    | —                      | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |   |
|   | 9.5                   | 0,10                   | —                      | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |   |
|   | 13.5                  | 0,15                   | —                      | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |   |
| Output Voltage: Low-Level, V <sub>OL</sub> Max                                      | —                     | 0,5                    | —                      | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |   |
|   | —                     | 0,10                   | —                      | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |   |
|   | —                     | 0,15                   | —                      | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |   |
| Output Voltage: High-Level, V <sub>OH</sub> Min                                     | —                     | 0,5                    | —                      | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |   |
|   | —                     | 0,10                   | —                      | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |   |
|   | —                     | 0,15                   | —                      | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |   |
| Input Low Voltage, V <sub>IL</sub> Max Note 1                                       | TTL-CMOS              | 1                      | —                      | 5                      | 10                                    | 0.8   |       |       |       | —                 | —    | 0.8   | V |
|   | TTL-CMOS              | 1                      | —                      | 5                      | 15                                    | 0.8   |       |       |       | —                 | —    | 0.8   |   |
|   | CMOS-CMOS             | 1                      | —                      | 5                      | 10                                    | 1.5   |       |       |       | —                 | —    | 1.5   |   |
|   | CMOS-CMOS             | 1.5                    | —                      | 5                      | 15                                    | 1.5   |       |       |       | —                 | —    | 1.5   |   |
|   | CMOS-CMOS             | 1.5                    | —                      | 10                     | 15                                    | 3     |       |       |       | —                 | —    | 3     |   |
| Input High Voltage, V <sub>IH</sub> Min Note 1                                      | TTL-CMOS              | 9                      | —                      | 5                      | 10                                    | 2     |       |       |       | 2                 | —    | —     | V |
|   | TTL-CMOS              | 13.5                   | —                      | 5                      | 15                                    | 2     |       |       |       | 2                 | —    | —     |   |
|   | CMOS-CMOS             | 9                      | —                      | 5                      | 10                                    | 3.5   |       |       |       | 3.5               | —    | —     |   |
|   | CMOS-CMOS             | 13.5                   | —                      | 5                      | 15                                    | 3.5   |       |       |       | 3.5               | —    | —     |   |
|   | CMOS-CMOS             | 13.5                   | —                      | 10                     | 15                                    | 7     |       |       |       | 7                 | —    | —     |   |
| Input Current, I <sub>IN</sub> Max  | —                     | 0,18                   | —                      | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |   |

Note 1: Applies to the 6 input signals. For mode control (P13), only the CMOS-CMOS ratings apply.

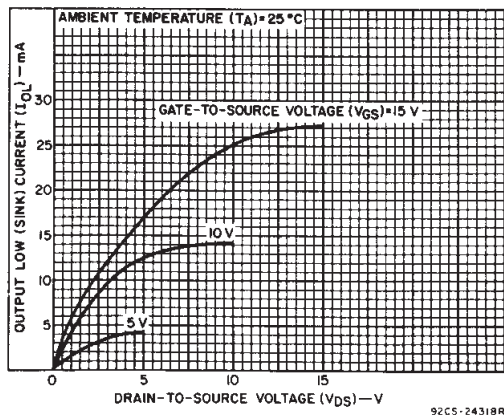


Fig. 2 - Typical output low (sink) current characteristics.

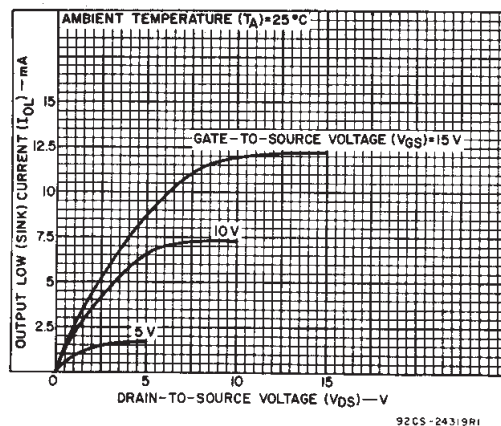
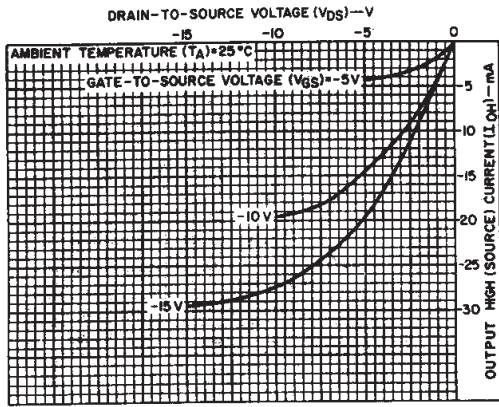


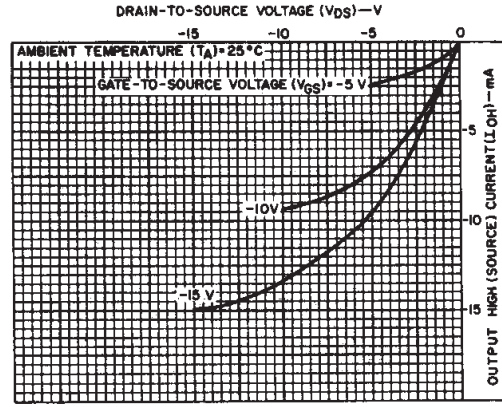
Fig. 3 - Minimum output low (sink) current characteristics.

# CD4504B Types



92CS-24320R3

Fig. 4 - Typical output high (source) current characteristics.



92CS-24321R2

Fig. 5 - Minimum output high (source) current characteristics.

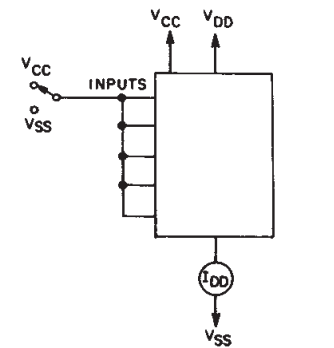
## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC   | V <sub>DD</sub> (V) | LIMITS |      | UNITS |
|--|---------------------|--------|------|-------|
|  |                     | Min.   | Max. |       |
| Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range) | —                   | 5      | 18   | V     |

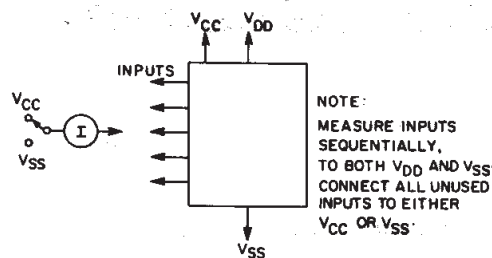
## DYNAMIC ELECTRICAL CHARACTERISTICS, At T<sub>A</sub> = 25°C; Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 Ω

| CHARACTERISTIC                                       | SHIFTING MODE                                     | V <sub>CC</sub> (V) | V <sub>DD</sub> (V) | LIMITS |      | UNITS |
|--|---|---------------------|---------------------|--------|------|-------|
|  |   |                     |                     | TYP.   | MAX. |       |
| Propagation Delay:<br>High-to-Low, t <sub>PHL</sub>  | TTL to CMOS<br>V <sub>DD</sub> > V <sub>CC</sub>  | 5                   | 10                  | 140    | 280  | ns    |
|  | CMOS to CMOS<br>V <sub>DD</sub> > V <sub>CC</sub> | 5                   | 15                  | 140    | 280  |       |
|  | CMOS to CMOS<br>V <sub>CC</sub> > V <sub>DD</sub> | 5                   | 10                  | 120    | 240  |       |
|  |   | 5                   | 15                  | 120    | 240  |       |
|  |   | 10                  | 15                  | 70     | 140  |       |
|  |   | 10                  | 5                   | 275    | 550  |       |
|  |   | 15                  | 5                   | 275    | 550  |       |
|  |   | 15                  | 10                  | 70     | 140  |       |
| Low-to-High, t <sub>PLH</sub>                        | TTL to CMOS<br>V <sub>DD</sub> > V <sub>CC</sub>  | 5                   | 10                  | 140    | 280  | ns    |
|  | CMOS to CMOS<br>V <sub>DD</sub> > V <sub>CC</sub> | 5                   | 15                  | 140    | 280  |       |
|  | CMOS to CMOS<br>V <sub>CC</sub> > V <sub>DD</sub> | 5                   | 10                  | 120    | 240  |       |
|  |   | 5                   | 15                  | 120    | 240  |       |
|  |   | 10                  | 15                  | 70     | 140  |       |
|  |   | 10                  | 5                   | 200    | 400  |       |
|  |   | 15                  | 5                   | 200    | 400  |       |
|  |   | 15                  | 10                  | 60     | 120  |       |
| Transition Time, t <sub>THL</sub> , t <sub>TLH</sub> | All Modes   |                     | 5                   | 100    | 200  | ns    |
|  |   |                     | 10                  | 50     | 100  |       |
|  |   |                     | 15                  | 40     | 80   |       |
| Input Capacitance, C <sub>IN</sub>                   | Any Input   |                     |                     | 5      | 7.5  | pF    |



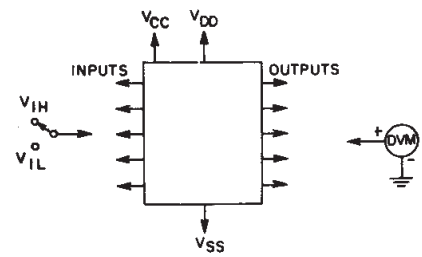
92CS-29452

Fig. 6 - Quiescent device current.



92CS-29454

Fig. 7 - Input current.



NOTE:  
TEST ANY COMBINATION  
OF INPUTS

92CS-29453

Fig. 8 - Input voltage.

3  
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# CD4504B Types

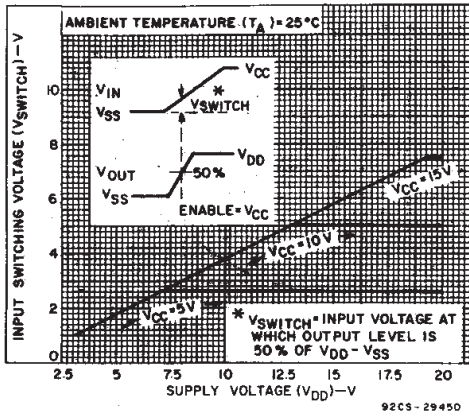


Fig. 9 - Typical input switching as a function of high-level supply voltage. (SELECT at  $V_{CC}$ -CMOS mode).

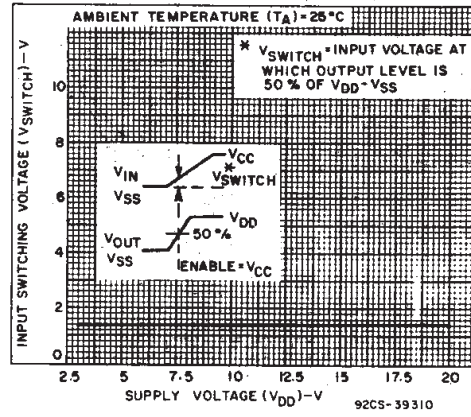


Fig. 10 - Typical input switching as a function of high-level supply voltage (SELECT at  $V_{SS}$ -TTL mode).

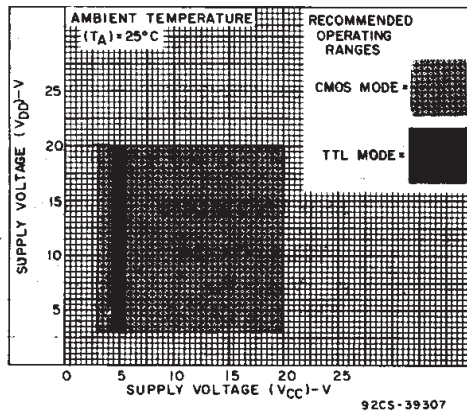
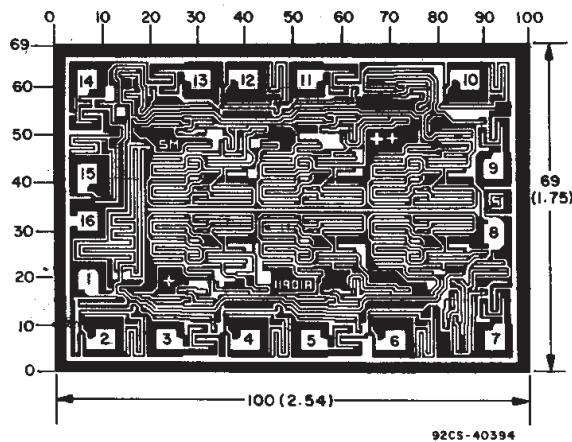


Fig. 11 - High-level supply voltage vs. low-level supply voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and pad layout for CD4504BH.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4504BE         | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD4504BEE4       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD4504BF3A       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| CD4504BM         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BM96       | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BM96E4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BM96G4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BME4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BMG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BMT        | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BMTE4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BMTG4      | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BPW        | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BPWE4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BPWG4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BPWR       | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BPWRE4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD4504BPWRG4     | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS

compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF CD4504B, CD4504B-MIL :**

- Enhanced Product: [CD4504B-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4504BM96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD4504BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4504BM96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD4504BPWR | TSSOP        | PW              | 16   | 2000 | 346.0       | 346.0      | 29.0        |



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

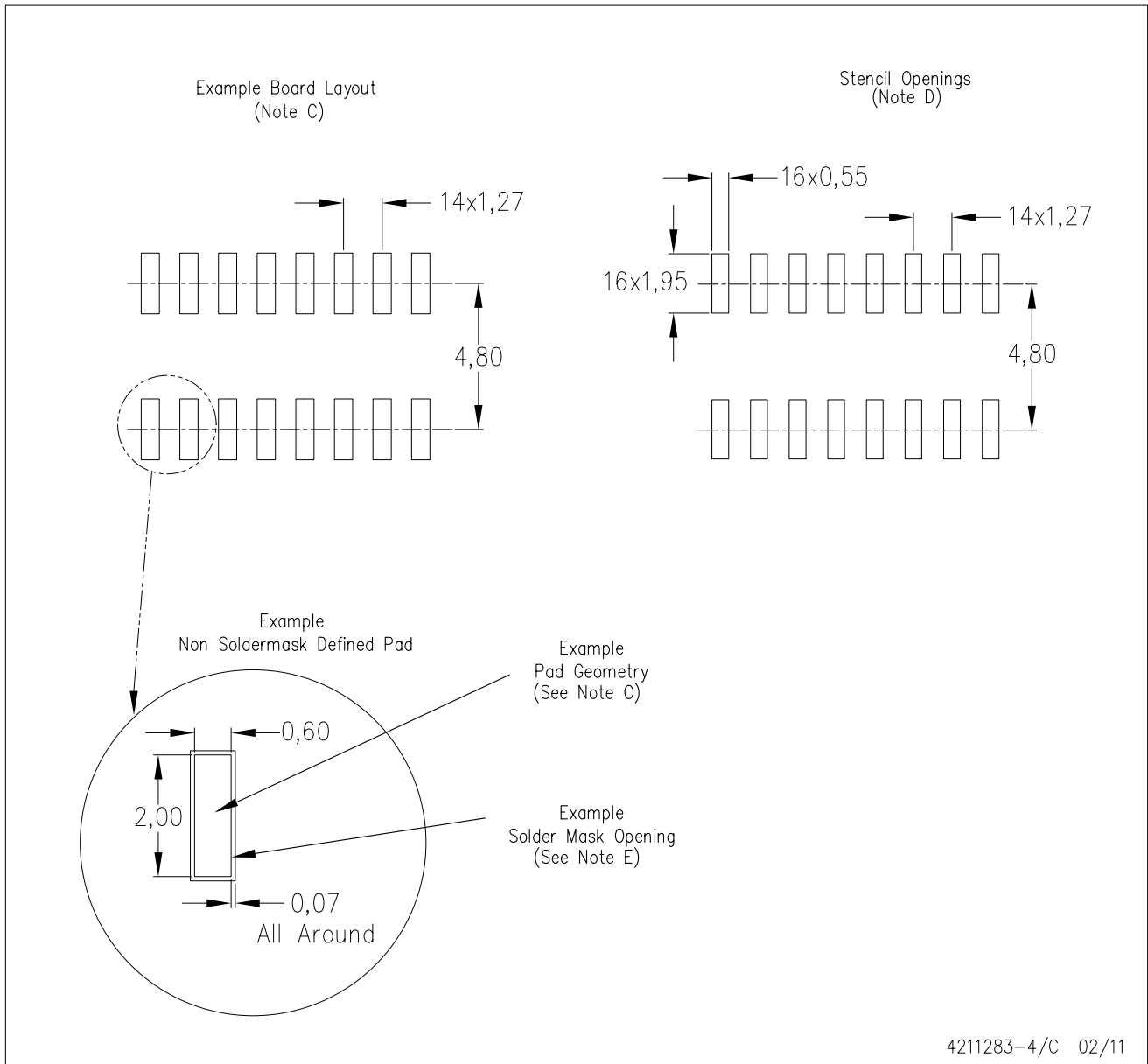


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

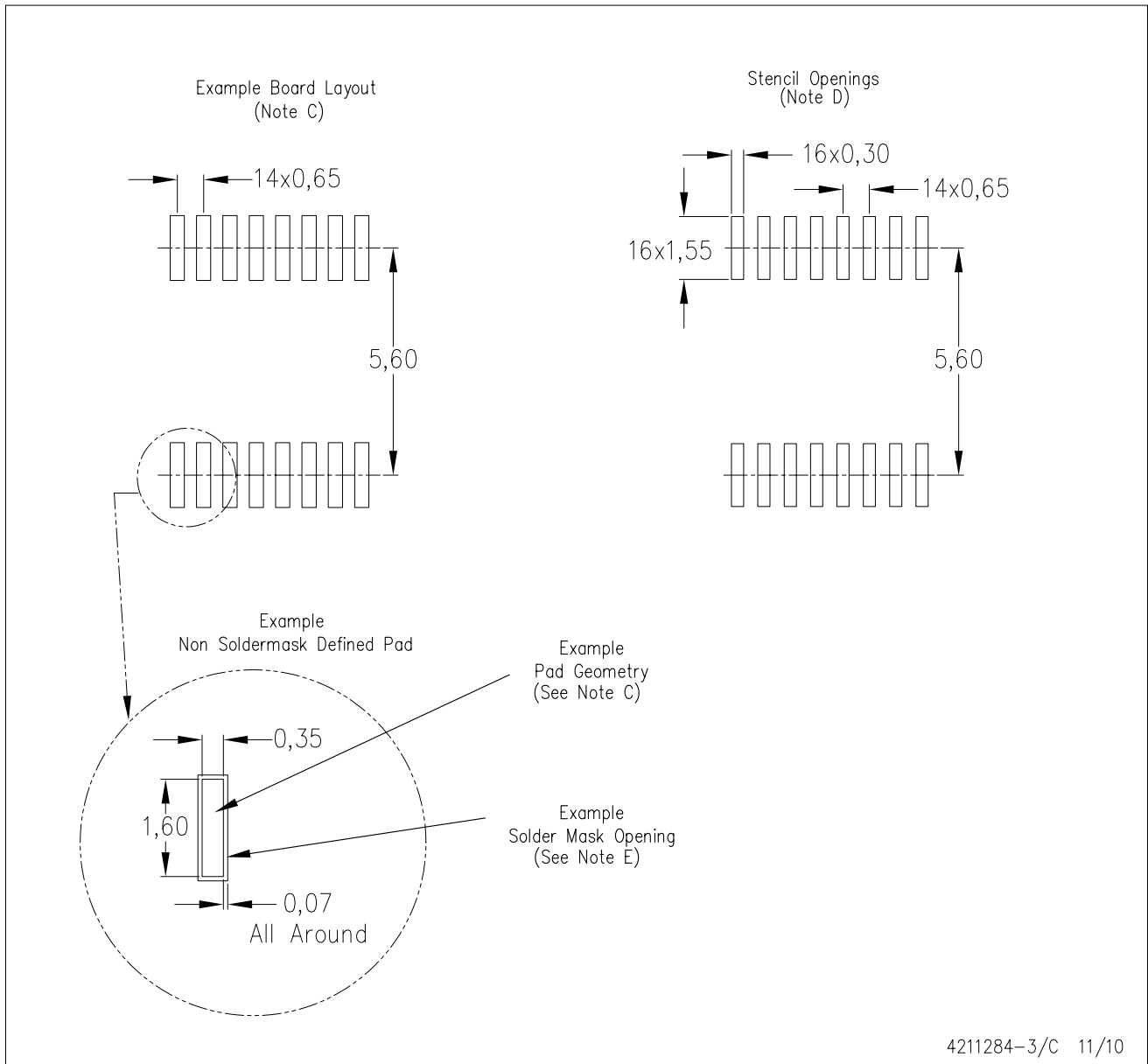


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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